CMOS-compatible 512kb SOT-MRAM with topological material (TL-RAM)

T. Kishi[1], M. Yamaguchi[1], H. Ohmori[1], H. Tanizaki[1], A. Hachisuka[1], S. Hamasaka[1], K. Kawabata[1], R. Akiyama[1], A. Yamazaki[1], T. Oishi[1], T. Higo[2], S. Nakatsuji[3,1]

[1]TopoLogic Inc., Tokyo, tatsuya_kishi@topologic.jp
[2]Faculty of Science and Technology, Keio University, Kanagawa
[3]Department of Physics, Graduate School of Science and Faculty of Science, The University of Tokyo, Tokyo

Abstract — We are developing spin-orbit torque (SOT-) MRAM using antiferromagnetic topological materials as the free layer, aiming for high speed and low power consumption. We successfully integrated for the first time a top-pinned perpendicular MTJ on an 8-inch wafer using a full-scale CMOS-compatible process. The fabricated chip is a 512kbit array with 100 nm MTJs. We used Mn3Sn, a topological noncollinear antiferromagnetic metal, as the free layer. Mn3Sn was deposited by sputtering on Ta-SOT and was confirmed to be sufficiently ordered by 400C annealing. Evaluation of single bits within the array showed hysteresis with a TMR of about 89%. The switching current density was 8.4 MA/cm² at 10 ns, significantly reduced compared to existing CoFeB free layers. The pulse-width dependence of the measured switching current density and that of the simulation suggested that switching is possible in the sub-nanosecond regime with a reasonable reversal current.

***Index Terms*—SOT-MRAM, Topological material, Magnetic tunnel junction, CMOS-compatible**

I. Introduction

Antiferromagnetic materials do not have stray magnetic fields, are resistant to external magnetic fields, and are expected to operate at high speeds in the terahertz range, which is why they have consistently attracted significant attention for device applications. However, in antiferromagnets, especially collinear antiferromagnets, detecting their magnetic state is extremely difficult, and to utilize collinearity, nearly perfect crystals are usually required. On the other hand, research on topological materials, which originated from Nobel Prize-winning work such as the quantum Hall effect and the theory of topological phase transitions, has become active. Topological materials are generally those whose electronic states are described by topological invariants, and various types of materials have currently been discovered. The material Mn3Sn [1] adopted in this study is classified as a Weyl semimetal among topological materials and is a non-collinear antiferromagnet in which magnetic Mn atoms form a kagome lattice, with a magnetic easy plane within the kagome plane. Furthermore, the presence of ferromagnetic order of higher-order cluster magnetic octupoles results in the manifestation of a giant anomalous Hall effect and magneto-optical Kerr effect [2], etc. Regarding magnetization dynamics, picosecond-order switching has been confirmed [3]-[4], and applications to memory devices operating at high speed and low power consumption are expected.

In this paper, we report on the development results of SOT-MRAM using Mn3Sn (TL-RAM), one of the topological non-collinear antiferromagnets. Mn3Sn itself is expected to allow picosecond switching, and high-speed SOT-switching is also expected as a device [5]-[6]; however, for readout, only small TMR has been experimentally reported in the tunnel junction Mn3Sn/MgO/Mn3Sn [7]. Theoretically, TMR exceeding 1000% is suggested due to momentum-dependent spin polarization on the Fermi surface [8], but it is necessary to ensure crystalline alignment at the interface, making it extremely difficult to realize in MTJs sputtered as poly-crystalline films on CMOS substrates. We aim to develop a memory device that can achieve both high-speed switching and large TMR, proposing an MTJ with Mn3Sn/CoFeB as the free layer, simultaneously including a tunnel junction of perpendicular magnetization CoFeB with MgO. A 512 kbit SOT-MRAM including the MTJ as a 1-bit cell was fabricated on an 8-inch wafer using a CMOS-compatible process. The characteristics of this SOT-MRAM were investigated.

II. Experiment

We prepared a 512kbit array as a vehicle for the development of TL-MRAM. This 512kbit array consists of 32 sub-arrays of 16kbit each (Fig. 1(a)). Each 1-bit cell contains two transistors, connected by a common bit line (Fig. 1(b)). The MTJ film was sputtered on an 8-inch CMOS wafer at the 180 nm node and then annealed at 400°C to order the Mn3Sn. The stack of the SOT-MTJ device basically consists of Ta, Mn3Sn/CoFeB, MgO, and CoFeB, as SOT-layer, free layer, insulator, and pinned layer, respectively (Fig. 2). A single perpendicular ferromagnetic layer was employed here as a pinned layer. The MTJ was formed with sizes of 80, 100, and 160 nm using electron beam lithography, and etched using ICP + milling, followed by SOT processing. In the MTJ processing, conditions were optimized to prevent redeposition on the sidewalls near MgO layer. The SOT width was set to a size expanded by 110 nm on both sides relative to the MTJ, taking alignment accuracy into consideration. For the evaluation of array operation, a home-made memory tester was used.

III. Results

First, we discuss the results of current writing for a typical single bit within the 512kbit array. Figure 3 shows the results of repeating current writing 10 times on the same 160nm-sized MTJ with an assist magnetic field Hx of 0.3 kOe. This device shows a TMR of 67% on average and 84% at maximum. The squareness of the hysteresis curves of this device is not so good. After the transition from the parallel state to the antiparallel state at positive current values, there is some fluctuation in the

antiparallel state resistance. This suggests that the MTJ size is large and includes multiple magnetic domains. This fluctuation is expected to be resolved by reducing the MTJ size to about 50nm or less. In addition, the switching current Ic was 571 μA. Considering a wide SOT with alignment taken into account, the current density is calculated as 7.5 MA/cm². Compared to reports on MTJs using CoFeB [10]-[11], the switching current density has been significantly reduced.

To investigate the high-speed switching of Mn3Sn, the switching current density was measured by varying the write pulse widths to 10, 20, and 50 ns, and 100 us for a 1-bit cell in the array. The results are shown in Figure 4. Over a wide range of 10 ns to 100 us, it is the area where thermal assistance is used to switch the area. The figure shows the simulation results for the thermal stability index Δ~33. For pulses shorter than 10 ns, CoFeB enters the precession region, causing a sharp increase in switching current. The results of this simulation are also illustrated in illustrations. However, in the case of Mn3Sn, no increase in switching current is observed up to the sub-nanosecond region [10]. The MTJ proposed here uses a free layer of Mn3Sn/CoFeB. In this case, the pulse width dependence of the switching current is expected to be the average dependency of Mn3Sn and CoFeB respectively. Therefore, even for a 1 ns write pulse, a significant increase in switching current may not occur. In other words, it could become a high-speed memory device with 1 nanosecond speed, comparable to SRAM.

IV. Conclusion

We have fabricated the world's first SOT-MRAM using MTJs (TL-RAM) that include topological materials. As the topological material, we used Mn3Sn, a non-collinear antiferromagnet. To achieve both the high-speed switching characteristics of Mn3Sn and a large TMR as an MTJ, we adopted a structure combining Mn3Sn with CoFeB as a free layer. Using this MTJ as a 1-bit cell, we fabricated a 512 kbit array as a memory device using a CMOS-compatible process. The 1-bit cell exhibited 89% of TMR, and the switching current density for a 10 ns write pulse was demonstrated to be 8.4 MA/cm². Regarding writing, simulations corresponding to Mn3Sn and CoFeB were performed, showing the potential for high-speed operation in the MTJ we proposed. In the future, by optimizing the MTJ structure and CMOS-compatible process, the feasibility of realizing even faster and lower power SOT-MRAM is suggested.

ACKNOWLEDGEMENT

This study is based on results obtained from a project, JPNP24011, subsidized by the New Energy and Industrial Technology Development Organization (NEDO).

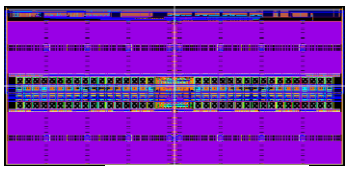

Figure 1(a)

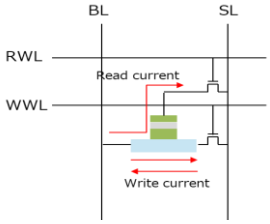

Figure 1(b)

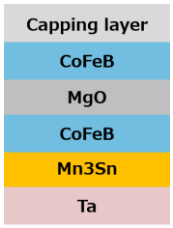

Figure 2

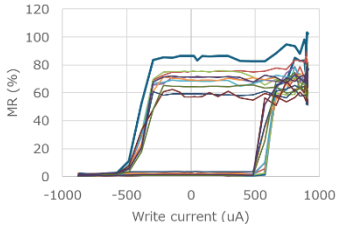

Figure 3

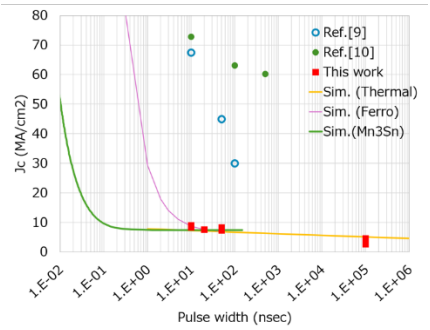

Figure 4

References

[1] S. Nakatsuji, *et al*, "Large anomalous Hall effect in a non-collinear antiferromagnet at room temperature," Nature, vol. 527, p. 212, 2015.

[2] T. Higo, *et al*., "Large magneto-optical Kerr effect and imaging opf magnetifg octupole domains in an antiferromagnetic metal," *Nature Photonics,* vol. 12, p. 73, 2018.

[3] S. Miwa, *et al*., "Giant Effective Danping of Octupole Oscillation in an Antiferromagnetic Weyl Semimetal," *Small Sci.,* vol. 1, p. 2000062, 2021.

[4] H. Tsai, *et al*., "Picosecond ultralow^power switching device based on an antiferromagnet," *Science,* vol. 392, p. 761, 2026.

[5] X. Chen, *et al.,* "Octupole-driven magnetoresitance in an antiferromagnetic tunnel junction," *Nature,* vol. 613, p. 490, 2023.

[6] T. Higo, *et al*., "Perpendicular full switching of chiral antiferromagnetic order by current," Nature, vol. 607, p. 474, 2022.

[7] Y. Takeuchi, *et al.,* "Electrical coherent driving of chiral antiferromagnet," *Science,* p. 830, 2025.

[8] K. Tanaka, *et al.,* "Ab initio study of magnetoresistance effect in Mn3Sn/MgO/Mn3Sn antiferromagnetic tunnel junction," Phys. Rev. Mater., vol. 10, p. 044405, 2026.

[9] K.-S. Li, *et al.*, "First BEOL-compativle, 10ns-fast, and Durable 55nm Top-pSOT-MRAM with High TMR (>130%)," *International Electron Devices Meeting (IEDM),* p.1, 2023.

[10] W. Yang, *et al.*, "Achieving High Yield opf Perpendicular SOT-MTJ Manufactured on 300 mm Wafers," *IEEE Electron Device Letters,* vol. 45, no. 11, pp. 2094, 2024.

[11] A. Shukla, *et al.*, "Impact of strain on the SOT-driven dynamicsof thin film Mn3Sn," *J. Appl. Phys.,* vol. 135, p. 12903, 2024.